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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,005	11/13/2003	Robert J. Campbell	DP-310085	1004
22851	7590	07/14/2005	EXAMINER	
DELPHI TECHNOLOGIES, INC. M/C 480-410-202 PO BOX 5052 TROY, MI 48007			WILLIAMS, ALEXANDER O	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/707,005

Applicant(s)

CAMPBELL ET AL

Examiner

Alexander O. Williams

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/13/03</u> | 6) <input type="checkbox"/> Other: ____ |

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Serial Number: 10/707005 Attorney's Docket #: DP-310085

Filing Date: 11/13/05;

Applicant: Cambell et al.

Examiner: Alexander Williams

This application is a continuation in part of application # 10/050344, filed 1/16/02.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The disclosure is objected to because of the following informalities: The continuation in part information should be updated.

Appropriate correction is required.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the at least two circuit devices between the first and second substrate members, each of the circuit devices having a first surface electrically contacting at least one of the electrically-conductive areas of the first substrate member, each of the circuit devices having a second surface electrically contacting a corresponding one of the electrically-conductive areas of the second substrate member in claim 1 and the first chip between the first and second

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substrate members, the first chip carrying a transistor having a gate electrode and a second electrode on a first surface thereof and a third electrode on an oppositely-disposed second surface thereof, the second electrode electrically contacting a first of the electrically-conductive areas of the first substrate member, the gate electrode electrically contacting a second of the electrically-conductive areas of the first substrate member, the third electrode electrically contacting a first of the electrically-conductive areas of the second substrate member; a second chip between the first and second substrate members, the second chip carrying a diode having a first electrode on a first surface thereof and a second electrode on an oppositely-disposed second surface thereof, the first electrode electrically contacting one of the electrically-conductive areas of the first substrate member, the second electrode electrically contacting a second of the electrically-conductive areas of the second substrate member; at least one lead electrically coupled to the first of the electrically-conductive areas of the first substrate member; at least one lead electrically coupled to the second of the electrically-conductive areas of the first substrate member; and at least one lead electrically coupled to the electrically-conductive areas of the second substrate member in claim 13 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure

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is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 1 to 20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear and confusing to what is meant by "at least two circuit devices between the first and second substrate members, each of the circuit devices having a first surface electrically contacting at least one of the electrically-conductive areas of the first substrate member, each of the circuit devices having a second surface electrically contacting a corresponding one of the electrically-conductive areas of the second substrate member." How are both sides of the devices electrically connected to the substrates? Where is this shown in the drawings?

In claim 13, it is unclear and confusing to what is meant by "the first chip between the first and second substrate members, the first chip carrying a transistor having a gate electrode and a second

electrode on a first surface thereof and a third electrode on an oppositely-disposed second surface thereof, the second electrode electrically contacting a first of the electrically-conductive areas of the first substrate member, the gate electrode electrically contacting a second of the electrically-conductive areas of the first substrate member, the third electrode electrically contacting a first of the electrically-conductive areas of the second substrate member; a second chip between the first and second substrate members, the second chip carrying a diode having a first electrode on a first surface thereof and a second electrode on an oppositely-disposed second surface thereof, the first electrode electrically contacting one of the electrically-conductive areas of the first substrate member, the second electrode electrically contacting a second of the electrically-conductive areas of the second substrate member; at least one lead electrically coupled to the first of the electrically-conductive areas of the first substrate member; at least one lead electrically coupled to the second of the electrically-conductive areas of the first substrate member; and at least one lead electrically coupled to the electrically-conductive areas of the second substrate member." Where is these connections, chips, electrodes etc.. shown in the drawings?

Any of claims 1 to 20 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

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The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/666,732,728,724,725,686,685,731,730,698,696,675,7 12,713,717,720	6/11/05
Other Documentation: foreign patents and literature in 257/666,732,728,724,725,686,685,731,730,698,696,675,7 12,713,717,720	6/11/05
Electronic data base(s): U.S. Patents EAST	6/11/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
7/11/05